3.7 Passive-Matrix Flexible Electronic Paper Using Quick-Response Liquid Powder Display (QR-LPD) Technology and Custom Driver Circuits

Reiji Hattori[1], Michihiro Asakawa[1], Yoshitomo Masuda[2], Norio Nihei[2], Akihiko Yokoo[2], Shuhei Yamada[2], Itsuo Tanuma[2]

[1]Kyushu University, Fukuoka, Japan
[2]Bridgestone, Tokyo, Japan

A new kind of electronic paper display is developed called Quick-Response Liquid Powder Display (QR-LPD®), which has a unique operational principle and special features such as a paper-like appearance, ultra-thin thickness, flexible and thin panel structure, and the ability to retain an image without power consumption [1].

Figure 3.7.1 shows the architecture and the operational principle of the QR-LPD. An appropriate amount of both white and black powder is sandwiched by ITO-patterned substrates with a gap of 50-100μm. A rib keeps the cell gap consistent and prevents the uneven distribution of powder between the pixels. Depending on an applied voltage, the charged particles switch places changing the color of appearance. These states are retained even if no voltage is applied due to the induced image and Van-der-Waals forces. This display can be driven by passive-matrix (PM) addressing because of clear threshold voltage characteristics and a high-speed response of less than 0.2ms.

Figure 3.7.2 shows the recently developed plastic panel with good flexibility, which has been partially fabricated by roll-to-roll fabrication. The thickness of this display is less than 300μm. Yellow, red, green and blue colors are also available as well as black and white colors using colored particles [2]. Another important function of QR-LPD is bistability. The image on a panel can be retained without power, even for several years. This feature dramatically decreases power consumption and opens new markets, such as price tags, electronic posters, and displays for IC cards. At the present stage, QR-LPD needs a relatively high driving voltage of up to 70V, which leads to high power consumption. Therefore, the development of a high-voltage and low-power consumption LSI driver is very important. The recently developed LSI driver has a long shape of 2.3mm×21.4mm and 160 outputs. The output requires a minimum of 3 voltage levels to apply the required low and high voltages with respect to the threshold voltage. A conventional CMOS process with the addition of a 110V LDMOS process was employed [3].

Figure 3.7.3 is a schematic view of the cross-sectional LDMOS structure. Since a triple-well structure is not available owing to the difficulty to form the pWELL surrounding the deep HV nWELL in a HV process of more than 40V, nMOS transistors cannot be used in floating mode. In addition, forming a thick gate insulator to withstand a HV of more than 40V is not possible at certain process cost points. Because of these limitations, a conventional circuit approach cannot be used to create a HV circuit operating with more than 40V, and thus a special circuit must be considered.

Figure 3.7.4 shows the schematic of a one output circuit where the level shifter has no bias circuit but the gate voltage swing of all HV pLDMOSs (H1-H5) or floating LV pMOSs (M1-M7) is restricted within the breakdown voltage of the thin gate insulator used in a digital part. The gate voltage swing is controlled by two diode-connected transistors (M5, M6) and the current is generated by the constant current source (I1, I2). To turn on the HV pLDMOSs (H1, H4, H5), the right side of the HV nLDMOS (H8) in the level shifter is opened by an on signal from the pulse generator circuit. After charging up the capacitance using the gate insulator of M7, H8 is closed immediately to prevent DC power dissipation. To turn off the HV pLDMOSs, H7 is first opened, turning M3 on and causing the gate voltage of the HV pLDMOSs to approach zero. DC power dissipation is avoided by a turn-off operation created by applying an off pulse. The characters G, M and H represent the voltage levels of ground, middle and high, respectively.

Figures 3.7.5 and 3.7.6 show the transient current waveforms that flow from the power sources of V_{DDH} and V_{DDM}, respectively, when a single output voltage changes. In this measurement, a 9.6cm×4.6cm sized panel with a 320×140 array was connected, and the supplied voltages were 70V and 35V for V_{DDH} and V_{DDM}, respectively. The panel capacitance fixed with a single output was measured by an impedance analyzer to be in the range of 2.4pF to 44pF depending on the measurement frequency. The energy consumed to charge this capacitance up to 70V should be in the range of 12nJ to 216nJ. Considering the current flow, the energy values of 68.5nJ and 46.6nJ in Fig. 3.7.5 are mainly consumed to charge up the panel capacitance while the energy value of 2.3nJ and 2.0nJ are consumed by the DC current in the level shifter. The large difference between these values reveals that our level shifter works well consuming a negligibly small amount of energy compared with that consumed in the panel while the conventional PDP driver consumes about 30nJ when it is used to drive our panel.

In the MV output, the energy consumed in the level shifter exceeds 8.6nJ as shown in Fig. 3.7.6. The reason for this is not clear yet, but it seems to arise due to complications related to the output circuit. Notice that no current is supplied during the transition M→H since the current for the level shifter is supplied from the V_{DDH}. In addition, the negative current flow can be observed during the transition H→M showing that some energy is recovered from the panel to the V_{DDM} power source. This recovered energy value is smaller than that expected by the energy value saved in the panel capacitance, which is due to the losses in the level shifter. However, this negative current flow shows clearly that energy recovery in the middle power source is possible if the power loss in the level shifter at MV can be substantially improved.

To achieve a flexible display including the driving circuit, the driving circuit must be mounted on the panel and have physical flexibility. Using flexible electronic technologies such as organic TFTs is one approach, however, they are still under investigation and are currently unsuitable for a PM-driven panel. In order to realize a physically flexible or bendable driving circuit, our custom driver LSI was successfully milled down to 35μm demonstrating good bendability as shown in Fig. 3.7.7. This ultra-thin driver LSI has already been confirmed to successfully drive the QR-LPD. This driver LSI will be mounted on a flexible QR-LPD directly and thus QR-LPD that looks like real paper can be achieved.

Acknowledgments:
The authors are indebted to I. Takeda, N. Tomita and Y Aoki of TOKO, Inc. for providing the HV CMOS/LDMOS process and beautiful work on thinning the chip.

References:
[1] Reiji Hattori et al., "A Novel Bistable Reflective Display using Quick-Response Liquid Powder," *Journal of SID,* vol. 12, no. 1, pp. 75-80, 2004.
[2] Ryo Sakurai et al., "Color and Flexible Electronic Paper Display using QR-LPD® Technology," *Proceeding of SID*, pp. 1922-1925, 2006.
[3] Reiji Hattori et al., "Three-Voltage-Level Driver for Quick-Response Liquid-Powder Display," *Proceeding of SID*, pp. 1410-1413, 2006.

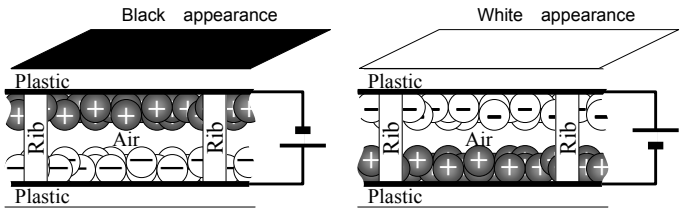

Figure 3.7.1: The QR-LPD architecture and the principle of operation.

Figure 3.7.2: PET base flexible QR-LPD.

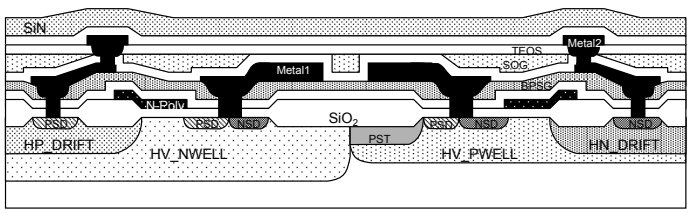

Figure 3.7.3: LDMOS cross-sectional view.

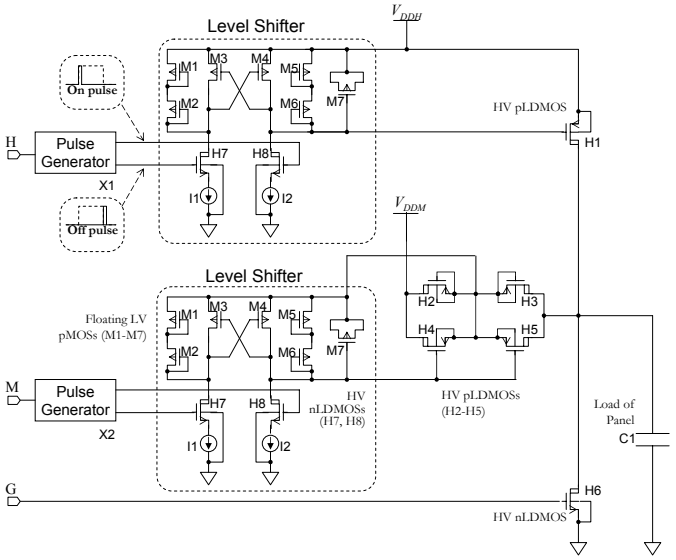

Figure 3.7.4: Output circuit with three-voltage levels.

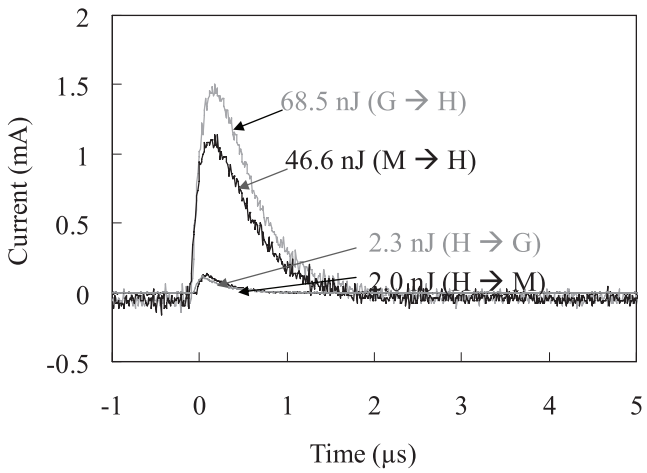

Figure 3.7.5: The transient current waveforms supplied from VDDH to the driver when a single output changes.

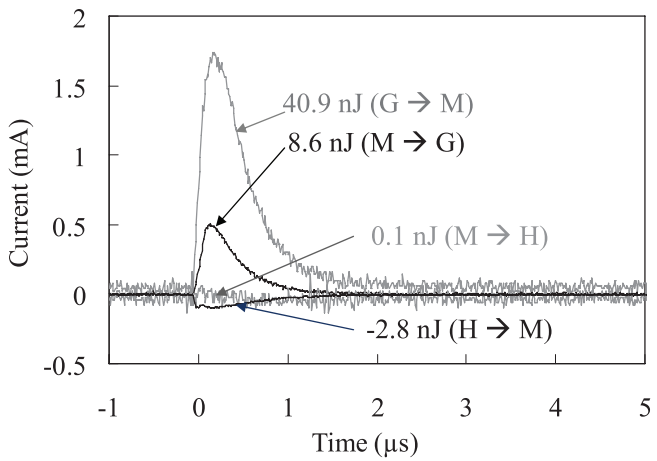

Figure 3.7.6: The transient current waveforms supplied from VDDM to the driver when a single output changes.

Continued on Page 588

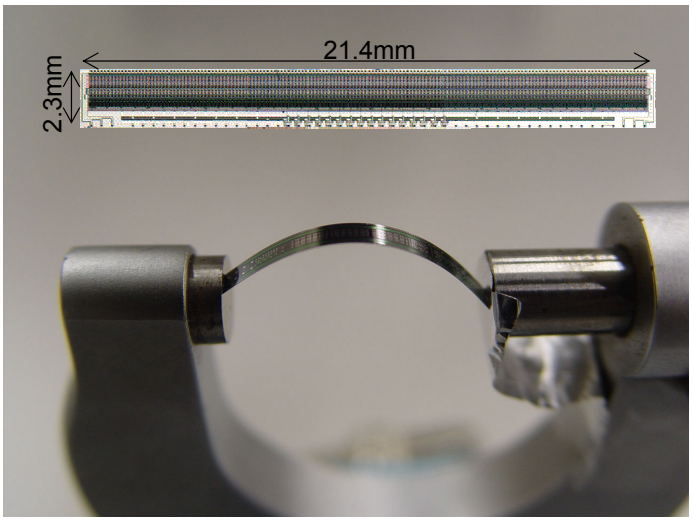

Figure 3.7.7: Ultra-thin and bendable driver LSI.

